IN THE SPECIFICATION

Please amend the specification on page 45, second full paragraph, as follows:

As shown, the control block 1880 has the signal input block 2110 for receiving an instruction Ext_CMD, a logical cell block address Ext_LBA and a local address Ext_RA from the external part and thereby ~~outputing~~ outputting a current instruction Cur_CMD, a current logical cell block address Cur_LBA and the current row address Cur_RA in the present execution clock and a previous instruction Pre_CMD, a previous logical cell block address Pre_LBA, a previous row address Pre_RA.

Please amend the specification on page 46, second full paragraph, as follows:

The clock delay block 2121 delays the inner restoration signal INTW[0:8] for one clock so that the inner restoration signal INTW[0:8] is later than the percharge active ~~singal~~ signal PC_ACT[0:8]. This is needed for restoring the data using the inner restoration signal INTW[0:8], after selecting the unit cell block using the precharge signal PC_ACT[0:8]; selecting one word line in the selected unit cell block; and sensing and amplifying the data in response to the selected word line.

Please amend the specification on page 64, first full paragraph, as follows:

In conclusion, when continuously reading in the same unit cell block, at first timing period, the memory device in accordance with the present embodiment amplifies the data in response to the inputted read instruction and the data is moved to the global bit line sense amplifier block, e.g., 2705A and 2705B and latched, at second timing period, the data latched in the global bit line sense amplifier block is moved to the unit cell block in which the predetermined word line of the word line activated by the read instruction and thereby restored.

Please amend the specification on page 71, fourth full paragraph, as follows:

Herein, the 'tBAT' is the converting time of the cell block address, the 'tRP' is the precharging time, the 'tRC' is the ~~privious~~ previous row cycle time, and the 'tINTW' is the restoration time by moving the internally latched data to the unit cell block of which word line is assigned as the predetermined word line.